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Code No: B0601

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II - SEMESTER EXAMINATIONS, APRIL/MAY 2012
DESIGN OF FAULT TOLERANT SYSTEMS
(DIGITAL SYSTEMS AND COMPUTER ELECTRONICS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Derive the reliability of a system in terms of reliabilities of the subsystems used to build it.
b) Define Maintainability and Availability and explain them clearly with relevance to a system.

2.a) Explain the importance of fault tolerance.
b) Explain the reliability of triple Modular redundancy.

3. Explain totally self-checking checker for Berger codes.

4. Explain fail safe design of sequential circuits using partition theory.

5.a) Explain Reed Mullar's expansion technique for testable combinational circuits.
b) Explain use of control and syndrome testable design technique for testable combinational circuits.

6.a) Explain theory and operation of LFSR.
b) Explain Signature analyzer.

7.a) Differentiate classic scan design and Level Sensitive Scan Design approaches.
b) Discuss advantages of Level Sensitive Scan Design Technique.

8.a) Discuss importance of BIST for VLSI chips.
b) Discuss various test pattern generations for BIST exhaustive testing with example.

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